REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-21 in the application. In a previous response, the Applicant amended Claims 1-2, 4-16 and 18-21. In the present response, the Applicant has amended Claims 1, 8 and 15 based on the recommendation of the Examiner. The amended claims do not necessitate a new search but further define the Claims and place the Claims in better condition for an appeal. No other claims have been amended or canceled. Accordingly, Claims 1-21 are currently pending in the application.

I. Rejection of Claims 1-6, 8-13 and 15-20 under 35 U.S.C. §103

The Examiner has rejected Claims 1-6, 8-13 and 15-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,532,579 to Sato, *et al.*, in view of U.S. Patent No. 6,681,354 to Gupta. The Applicant respectfully disagrees.

Sato does not teach or suggest an integrated circuit (IC) including a plurality of redundant hard macrocells as recited in independent Claims 1, 8 and 15. Instead, Sato teaches a semiconductor chip with circuit blocks that are each prepared for a single function (*i.e.*, a CPU, a DSP, a DRAM, *etc.*). Sato provides not teaching or suggestion of redundant circuit blocks. (*See* column 12, lines 47-57 and Figures 12 and 15.) In fact, Sato teaches away from having redundant circuit blocks since Sato is directed to preventing an increase in chip size. (*See* column 1, lines 45-47.) Accordingly, Sato teaches away from having "redundant hard macrocells" as recited in Claims 1, 8 and 15.

Additionally, even if Sato does teach or suggest an IC including "redundant hard macrocells," Sato provides no teaching or suggestion of an IC including a self-repair program that causes a programmable logic block to test at least some of a plurality of redundant hard macrocells and

place at least a functioning one of the plurality of redundant hard macrocells into an operational status as recited in Claims 1, 8 and 15. Instead, Sato teaches configuring programmable logic cells that exist between circuit blocks as repairing circuits for mending a faulty portion that exists in any of the circuit blocks. (*See* column 2, lines 53-56.) Thus, Sato teaches using programmable logic cells as repairing circuits for mending faulty portions of circuit blocks but provides no teaching or suggestion that the repairing circuits place a functioning circuit block into an operational status. Thus, Sato neither teaches nor suggests an IC including a plurality of redundant hard macrocells or a self-repair program as recited in independent Claims 1, 8 and 15.

As recognized by the Examiner, Sato also does not teach or suggest a programmable logic block. (*See* Examiner's Final Rejection, page 5.) To cure this deficiency of Sato, the Examiner cites Gupta. Gupta is directed to system-on-a-chip (SoC) devices that include an embedded field programmable gate array (FPGA) circuit that performs built-in self-test (BIST) functions. (*See* column 1, lines 8-12.) Gupta discloses a SoC device having components that are each configured for a particular function. (*See* column 4, lines 18-27, lines 40-48 and Figure 1.) Gupta does not teach or suggest a plurality of redundant hard macrocells as recited in independent Claims 1, 8 and 15. Thus, Gupta also does not teach or suggest a self-repair program that places at least a functioning one of the plurality of redundant hard macrocells into an operational status as recited in Claims 1, 8 and 15. Accordingly, Gupta does not cure the above deficiencies of Sato.

Thus, the cited combination of Sato and Gupta, individually or in combination, fails to teach or suggest a plurality of redundant hard macrocells or a self-repair program as recited in independent Claims 1, 8 and 15. Accordingly, the cited combination of Sato and Gupta does not provide a *prima facie* case of obviousness of Claims 1, 8 and 15 and Claims dependent thereon. As

such, Claims 1-6, 8-13 and 15-20 are not unpatentable in view of the cited combination. Therefore, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-6, 8-13 and 15-20 and allow issuance thereof.

Moreover, the Applicant reiterates that one skilled in the art would not be motivated to combine Sato and Gupta since neither reference provides a motivation for combining. Sato is directed to providing an IC having a self-examining test circuit that can be configured without an increase in chip size. (*See* column 1, lines 45-47.) To achieve this, Sato uses programmable cells in between circuit blocks. (*See* column 2, lines 20-27.) Gupta, on the other hand, teaches an embedded FPGA that can be used for testing other embedded circuit components of an integrated processing system. (*See* Abstract.) Thus, Gupta teaches a dedicated, embedded FPGA that is configured to perform BIST (*see* column 1, line 66 to column 2, line 4) while Sato teaches against such an embedded FPGA by employing programmable logic cells in free space to reduce chip size (*see* column 2, lines 20-31). Accordingly, neither Sato nor Gupta provide motivation for combining thereof.

II. Rejection of Claims 7, 14 and 21 under 35 U.S.C. §103

The Examiner has rejected Claims 7, 14 and 21 under 35 U.S.C. §103(a) as being unpatentable over Sato and Gupta in further view of U.S. Patent No. 5,638,382 to Krick, *et al.* The Applicant respectfully disagrees. As argued above, the cited combination of Sato and Gupta does not teach or suggest each element of independent Claims 1, 8 and 15. Krick has not been cited to cure the deficiencies of Sato and Gupta but to teach the subject matter of dependent Claims 7, 14 and 21. Thus, the cited combination of Sato, Gupta and Krick fails to

teach or suggest each element of independent Claims 1, 8 and 15 and Claims dependent thereon. Accordingly, the cited combination of Sato, Gupta and Krick does not provide a *prima facie* case of obviousness of Claims 1, 8, and 15 and Claims 7, 14 and 21 which depend thereon, respectively. Therefore, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 7, 14 and 21 and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-21.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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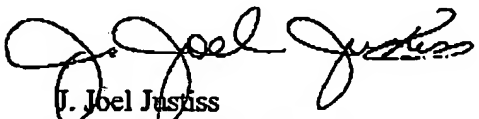

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